EK-OTM78-UG-001

TM78

Magnetic Tape Formatter User Guide

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CONTENTS

FIGURES

TABLES

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The TM78 Magnetic Tape Formatter serves as an interface between a maximum of four TU78 Magnetic Tape Transports and any MASSBUS controller. It provides control, data, status, and error information between the MASSBUS controller and the standard 1.27 cm (0.50 in) TU78 Tape Transport, operating at 318 cm/sec (125 in/sec). The TM78 can read and write magnetic tape for information interchange at 1600 bits/in phase encoded (PE) or 6250 bits/in group-coded recording (GCR). It also has spacing and reverse read capabilities. The TM78 formats data from PDP-11 family, DECsystem-10, DECSYSTEM-20 and VAX processors into tape frame characters, and performs the reverse during a data read operation.

Aside from magnetic tape formatting, the TM78 offers the following features.

1. Automatic two-track error correction when reading GCR data
2. Resident on-line microdiagnostics
3. Full wraparound maintenance diagnostics
4. Dual MASSBUS port capability
5. Automatic transport velocity monitoring
6. Programmable self-diagnosing facility
7. Full data path parity checking
8. Automatic single-track error correction when reading PE data
9. Automatic error repositioning for retries

1.2 GENERAL DESCRIPTION

Figure 1-1 illustrates a TM78/TU78 tape transport system configuration. Up to four TU78 tape transports can interface with one TM78 tape formatter. Each transport is independently cabled using a radial bus configuration. Thus, one or more transports can be removed while the others remain on-line.

Each MASSBUS controller can control up to eight TM78 formatters. Thus, a maximum of 32 TU78 tape transports could interface with a single MASSBUS controller.

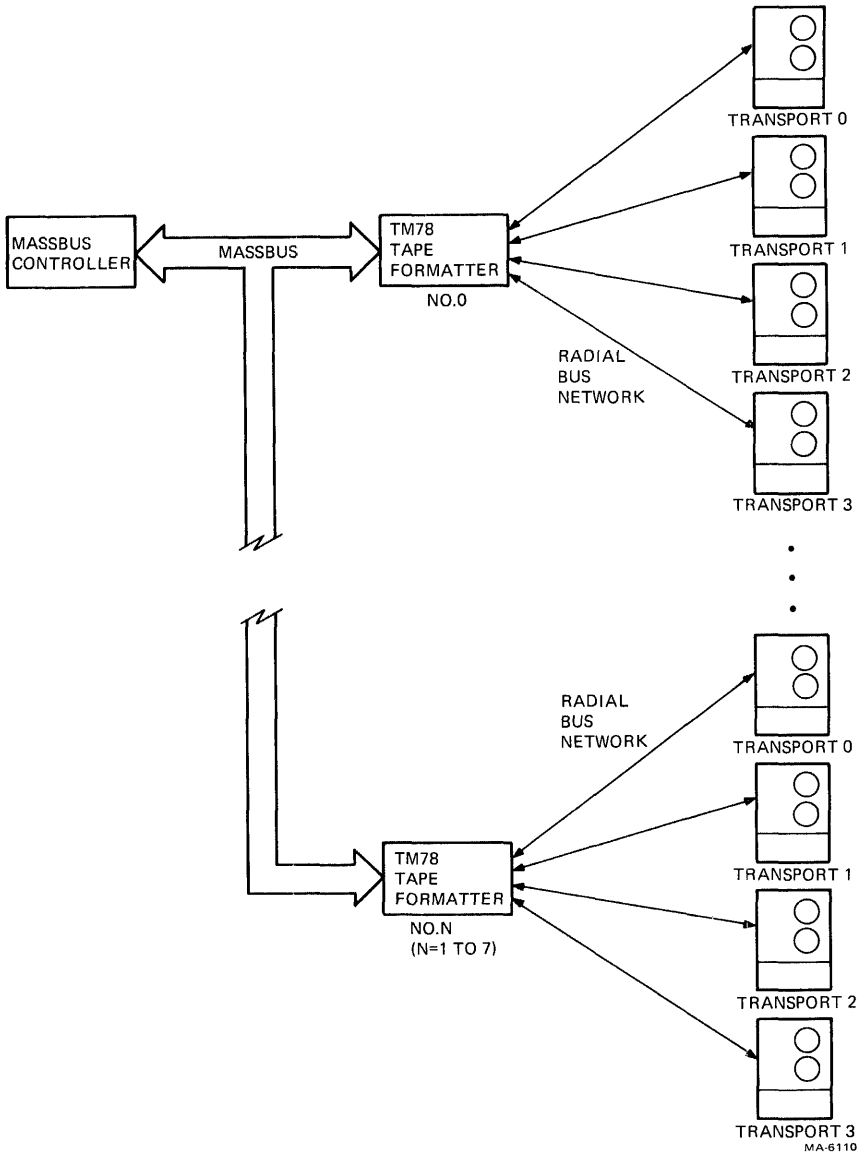


Figure 1-1 TM78/TU78 Tape Transport System Configuration

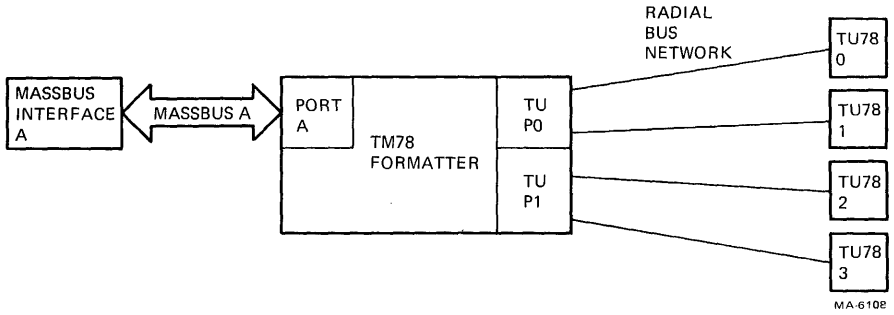


Figure 1-2 TM78-AB Subsystem Configuration

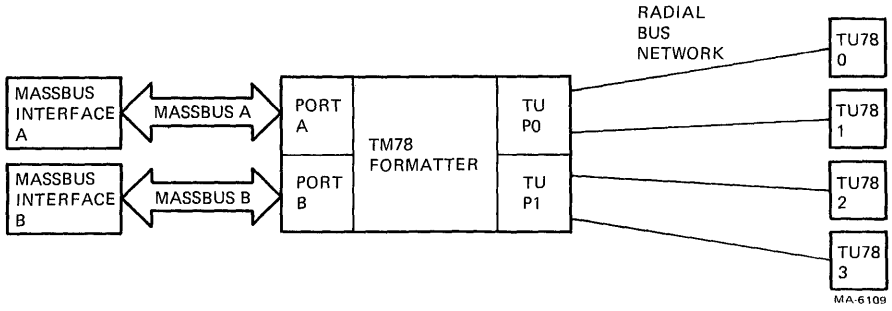


Figure 1-3 TM78-BB Subsystem Configuration

1.2.1 Options

The list below briefly describes all available TM78 options.

Option No	TM78 Configuration
TM78-AB	Single port TM78 capable of interfacing with single MASSBUS and up to four TU78s (Figure 1-2)
TM78-BB	Dual port TM78 capable of interfacing with two MASSBUSes and up to four TU78s (Figure 1-3)
TM78-C	Dual port adapter kit for TM78-AB

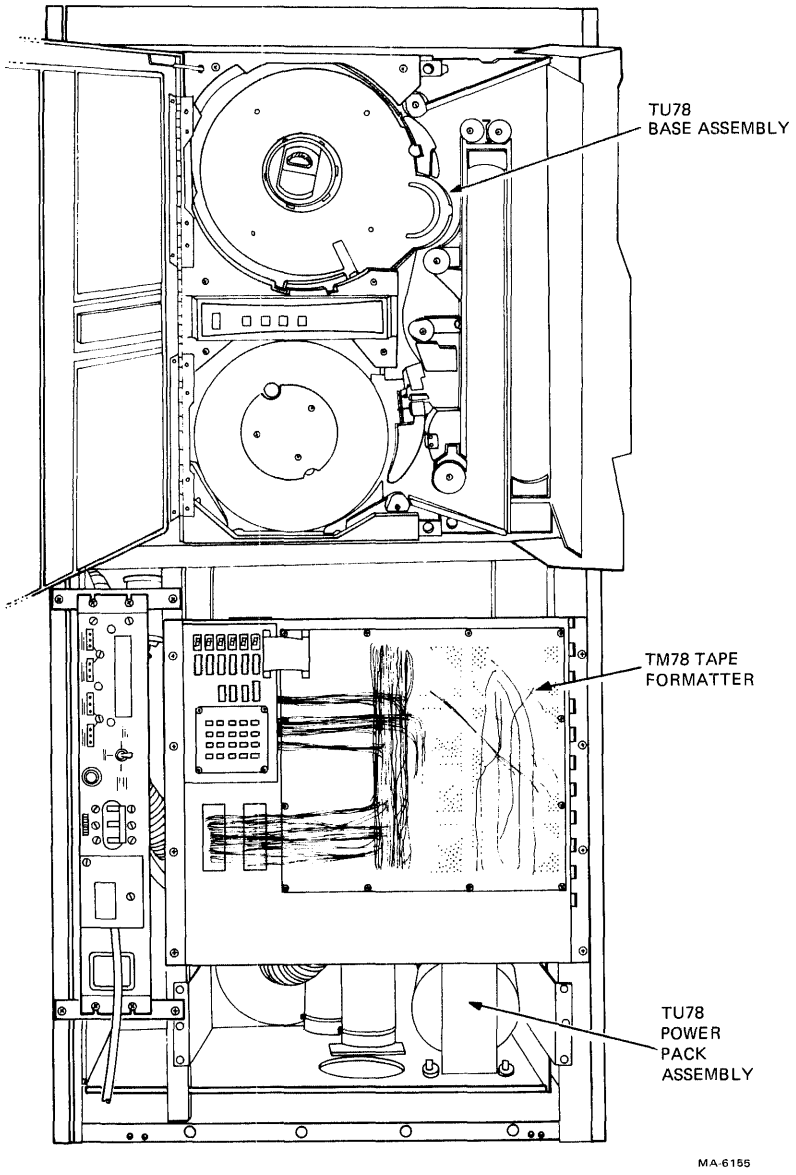


Figure 1-4 TM78 Mounted in Master TU78

1.2.2 Physical Description

Figure 1-4 shows the TM78 mounted within the master TU78 tape transport cabinet. An H7422-AB power supply provides power for the TM78, and is mounted in the rear of the master cabinet. Major subassemblies of the TM78 are the H7422-AB plus regulators (PN 70-17121) and TM78 tape formatter logic gate. Figure 1-5 shows the front view of the TM78.

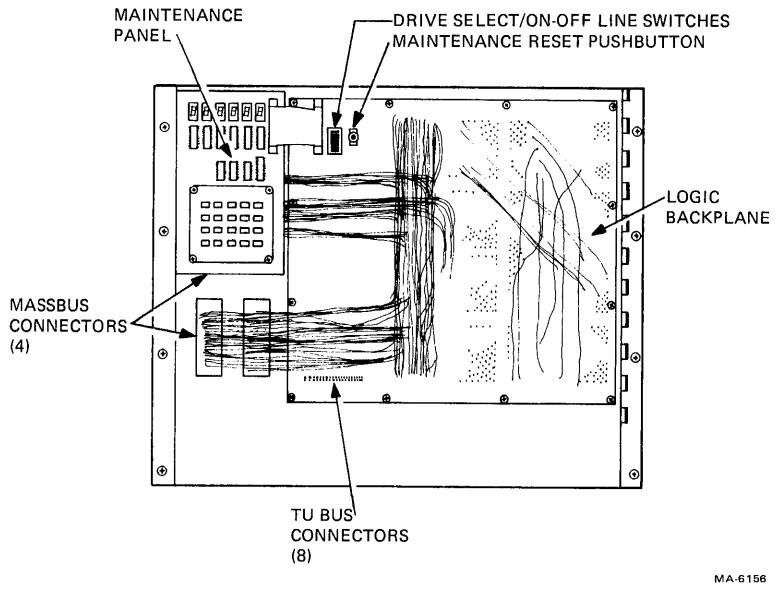


Figure 1-5 TM78 Front View

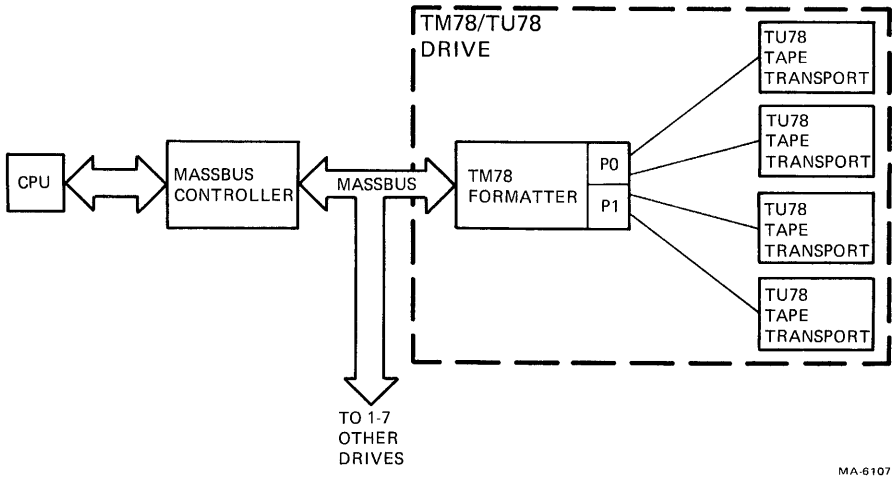


Figure 1-6 TM78 System Configuration

1.3 FUNCTIONAL DESCRIPTION

The TM78/TU78 tape transport system (Figure 1-6) interfaces with the central processor unit (CPU) via the MASSBUS controller. However, the MASSBUS controller is almost transparent to the CPU; that is, the CPU operates as though it controls the drive directly. (Throughout this manual, drive refers to a complete tape subsystem, comprising a TM78 tape formatter and a TU78 tape transport.)

The TM78 interfaces with the MASSBUS controller via the MASSBUS. The MASSBUS consists of an asynchronous control bus and a synchronous data bus, both with associated control lines. Transactions on the control bus control the drive and determine its status, while transactions on the data bus transfer data to or from the drive. Because the data and control buses operate independently, the MASSBUS controller can monitor drive status during a data transfer operation.

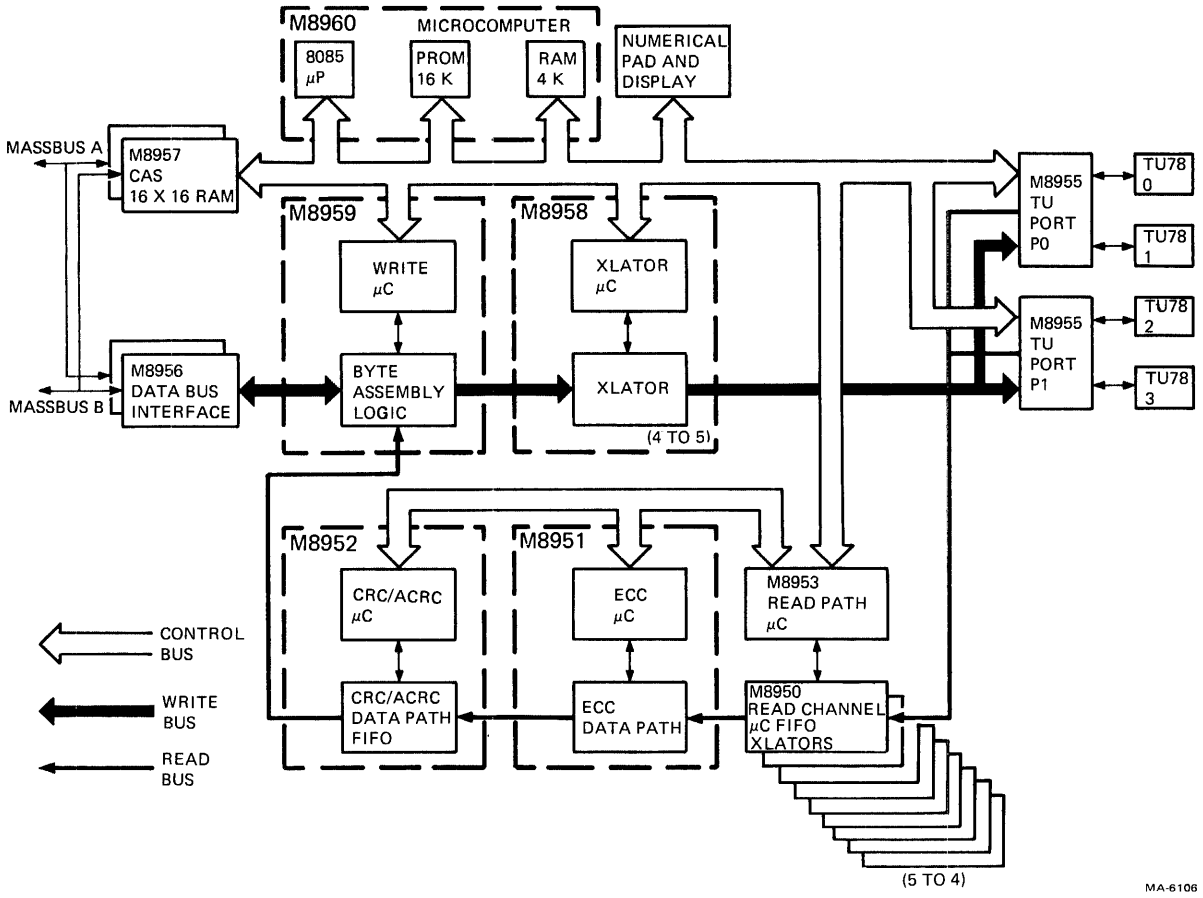


Figure 1-7 TM78 Simplified Block Diagram

The TM78 can control up to four tape transports through its dual port/radial bus scheme. Each tape unit bus (radial bus) cable set is identical with one tape transport per cable set to the formatter. The bus consists of write data, read data, control and various transport status lines.

1.3.1 System Operation

Figure 1-7 is a block diagram of the TM78, showing the major functional groups, control lines, and data paths. The following paragraphs describe these functional groups. While reading them, keep in mind that the word system implies the TM78 microcomputer system, and not some other portions (e.g., VAX, 11/70) or an overall computer system also run under microcode.

1.3.1.1 Common Address Space (M8957) – The common address space (CAS) interfaces the TM78 with the MASSBUS controller. It contains circuitry that decodes the drive select signals on the MASSBUS. Enabled by the proper drive select address code, the CAS module can carry on handshake operations with the MASSBUS controller, reading and writing TM78 registers.

Two TM78 registers provide a direct path from the MASSBUS to TM78 hardware. These registers are used for initialization, loading and verification of diagnostic microcode, starting and stopping the microprocessor, and diagnostic register access. The most important parts of the two registers are internal address and internal data.

The system microcomputer decodes command information in CAS registers and generates appropriate control signals to the transport. The module/microcode (that is, the microcode within the module) also determines when to perform a data transfer operation. When this is the case, it generates OCC (occupy) on the MASSBUS to notify the controller that it has occupied the data bus.

1.3.1.2 Data Bus Interface (M8956) – The data bus interface module interfaces the TM78 data paths with the MASSBUS controller.

The data bus interface is enabled for operation when the MASSBUS controller signal OCC is asserted. During a write operation, the MASSBUS controller places a data word on the data bus. When the data bus interface is ready to accept this data word, it asserts S CLK (sync clock) to the controller, which then replies with W CLK (write clock).

After receiving W CLK, S CLK is negated and the data bus interface strobes in the 18-bit word on the data bus. After generating W CLK, the MASSBUS controller places the next data word on the data bus. When the data bus interface module completes transferring the previous data word to the byte assembly logic (M8959), it issues another S CLK, receives another W CLK, and strobes in the next data word for transfer. The process continues until all data has been transferred (providing there are no data errors or other failures).

During a read operation, the data bus interface module receives an 18-bit word from the byte assembly logic. It is placed on the data bus, along with a parity bit (D PAR), and the data bus interface generates an S CLK pulse. When the MASSBUS controller receives S CLK, it strobes in the data on the data bus. The data bus interface module continues to receive 18-bit data words, and notifies the controller that a data word is available by generating S CLK. As in a write operation, the method of word/character assembly is under complete control of the system microcode.

1.3.1.3 Write Micro/Byte Assembly (M8959) – The write micro/byte assembly module is a ROM microcontroller dispatched on various tasks and monitored by the system microcomputer (M8960). In addition to allowing diagnostic data injection to the write logic during diagnostic testing, the write micro portion of the module functions in both write and read modes.

Write Mode

1. Receives data from MASSBUS data module
2. Disassembles data for translator in one of seven formats
3. Checks data parity from MASSBUS
4. Generates data parity to translator
5. CRC character calculation
6. ECC character calculation (GCR)
7. ACRC character calculation (GCR)
8. Formats residual and CRC data groups (GCR)

Read Mode

1. Receives data from read logic
2. Assembles data for MASSBUS in one of seven formats
3. Generates data parity to MASSBUS
4. Checks data parity from read logic
5. Facilitates data byte skip count

1.3.1.4 Write Translator (M8958) – The write translator is a ROM microcontroller initialized by the system microcomputer (M8960). Once initialized, it is controlled by the write micro portion of the M8959 module. The write translator contains a microprogram ROM, subgroup buffers, translation

ROMs, and control logic required to translate 4-bit data bytes into the 5-bit characters required in GCR formatting. In general, during a GCR write operation, this module performs the following functions.

1. Generates preamble and postamble
2. Performs 4 to 5 translation
3. Generates resync burst
4. Generates end mark
5. Controls flux reversal rate
6. Provides track enable/disable functions
7. Writes all ones

The module also performs the following functions during PE write operations.

1. Generates preamble and postamble
2. Controls flux reversal rate
3. Provides track enable/disable functions

1.3.1.5 System Microcomputer (M8960) – The system microcomputer module uses an 8085 microprocessor chip to act as the heart of the TM78 control bus (microbus). PROM space contains the operating system and diagnostic monitors. Specific diagnostic routines are loaded from the host computer system into 4K of additional RAM spaces before they are run.

The microcomputer directs TM78 operation over the TM78 microbus. it interfaces with the host CPU through the data bus interface and the CAS (common address space). The microcomputer's addressable memory space extends to the CAS. In this context, they form a tightly coupled asymmetrical multiprocessor system.

1.3.1.6 Tape Unit Port (M8955) – The tape unit port module interfaces the TM78 formatter with the tape transport. Two tape unit port modules may be used in each TM78 formatter, each module interfacing with two TU78 tape transports. During a TM78 write operation, the tape unit port module accepts either GCR or PE formatted data from the M8958, and transmits it to the tape transport to be written onto tape. Under complete microprogram control, bits in a TU command word inform the tape transport as to what format the proceeding data is in.

During TM78 read or write operations, the tape unit port module accepts either GCR or PE data. This time the data is to the TM78 from the tape transport. Again, the TU command word defines the data format.

This module also performs the following functions when the TM78 is running in diagnostic mode.

1. Loops translator to microcomputer
2. Loops translator to read path
3. Loops microcomputer to read path
4. Loops transport command register to transport status register
5. Loops microcomputer to AMTIE (amplitude track in error) lines
6. Loops AMTIE lines to microcomputer
7. Loops read data to microcomputer

1.3.1.7 Read Channel Module (M8950) – Nine read channel modules are used in the TM78 formatter, one for each tape track. Read channels are ROM microcontrollers, dispatched and monitored by the read path microcontroller (M8953). Read information feeds through the read channels, read data path, byte assembly, and data bus interface to the MASSBUS, and on to the CPU. During the read-after-write portion of the write cycle, information goes only as far as read data path logic, where ECC and CRC/ACRC checking are performed.

Basically, functions of the M8950 module during PE read/write operation are as follows.

1. Searches for preamble
2. Passes data to ECC
3. Deskews data
4. Read reverse correction
5. Verifies PE flux reversal

The main function of the module during GCR read/write operation is to translate the 5-bit GCR formatted data back into the original 4-bit format. Additional functions are as follows.

1. Searches for Mark 1
2. Passes data to ECC
3. Deskews data
4. Read reverse correction
5. AMTIE signal detection
6. TIE pointer generation

1.3.1.8 Read Path Controller (M8953) – The read path controller is a ROM microcontroller, dispatched and monitored by the system microcomputer. The read path dispatches and controls the nine read channel modules (M8950), and provides control information for the microcontrol portion of the ECC module. This module also serves as a central area of status reporting for the entire read electronics (read channels, ECC, and check character microcontroller parts).

The basic module functions for the respective formatter operations are listed below.

Write PE

1. Tests IRG (inter-record gap)
2. Tests ID Burst
3. Tests Tape Mark
4. Read-after-write

Write GCR

1. Tests IRG
2. Tests ID
3. Tests Tape Mark
4. Tests ARA ID
5. Tests ARA Burst
6. Read-after-write

Read GCR

1. Reads GCR forward
2. Reads GCR reverse
3. Samples density at BOT
4. Detects ARA ID
5. Detects Tape Mark

Read PE

1. Reads PE forward
2. Reads PE reverse
3. Samples density at BOT
4. Detects Tape Mark

Diagnostic Mode

1. Self tests diagnostic
2. Status register test
3. Load/read FIFO data

1.3.1.9 ECC Controller (M8951) – The ECC (error correcting code) controller module is a ROM microcontroller initialized by the system microcomputer, and thereafter controlled by the read path (M8953). This microcontroller implements the error-correction algorithms in both GCR and PE data formats, and in both read and write modes.

Read PE

1. Single track error correction

Write/Read GCR

1. Single track error correction always
2. Double track error correction with pointers

1.3.1.10 Check Character Controller (M8952) – The check character (CRC and ACRC) controller module is a ROM microcontroller initialized by the system microcomputer, and thereafter controlled by the ECC controller (M8951). This microcontroller performs check character algorithms in both read and write modes, PE and GCR data formats.

Write GCR

1. Verifies CRC and ACRC check characters

Read GCR

1. Verifies CRC and ACRC check characters
2. Passes data to byte assembly logic (M8959)

Write PE

1. Generates CRC verification character

Read PE

1. Passes data to byte assembly logic (M8959)

1.3.1.11 TM78 Maintenance Panel – A maintenance panel, consisting of pushbuttons and LED indicators, is provided to enhance subsystem troubleshooting. The maintenance panel is tied to the resident microcomputer and permits inspection of the formatter and transport without disabling the host CPU.

The panel keyboard/display is controlled exclusively by the TM78 microcode. The display remains blank until the ENA key is pressed, and recognized by the microcode; at that time, the LEDs display HELLO. The keyboard is enabled and all the keys may be used.

Subsystem failures and keypad operator errors generate a failure code (number) indicatd by the LEDs. The failure codes and associated subcode listings define the particular error or problem. This aids maintenance personnel, permitting them to work with one transport off-line, while the rest of the system remains on-line. Refer to Paragraph 5.5 of the *TM78 Technical Manual* for detailed information.

1.4 RELATED DOCUMENTS

The following list describes documents related to the TM78 formatter.

Title	Doc No	Contents
PDP-11 Peripherals Handbook	–	Register descriptions for RH MASSBUS controllers
RH10 MASSBUS Controller Maintenance Manual	EK-RH10-MM-002	Theory and maintenance of RH10 MASSBUS controller
RH20 MASSBUS Controller Unit Description	EK-RH20-UD-001	Description of RH20 MASSBUS controller
RH780 MASSBUS Adapter Technical Description	EK-RH780-TD-001	Programming and theory of RH780 MASSBUS adapter
TM78 Field Maintenance Print Set	MP01061	Engineering drawings and parts lists for TM78 mechanics and logic
H7422 Field Maintenance Print Set	Part of MP01061	Engineering drawings and parts lists for TM78 power supply chassis
H7441 Field Maintenance Print Set	Part of MP01061	Engineering drawings and parts lists for +5 volt regulator
H7476 Field Maintenance Print Set	Part of MP01061	Engineering drawings and parts lists for ±15 volt regulator
H7490 Field Maintenance Print Set	Part of MP01061	Engineering drawings and parts lists for −5 volt regulator

1.5 SPECIFICATIONS

Data Transfer Speed	780,000 char/sec maximum
Error Detection	
PE	Single track error correction
GCR	Single track error correction always; Double track error correction with pointers; CRC/ACRC check character verification
Maximum record length	65,536 characters (PE and GCR)

Minimum record length	1 character (PE and GCR)	
Environment		
Operating	10° C (50 °F) to 40° C (104 °F) 10 to 90 percent relative humidity Wet bulb: 28° C (82 °F) maximum Dew point: 2° C (36 °F) minimum	
Nonoperating	−40° C (−40 °F) to 66° C (151 °F) 0 to 95 percent relative humidity	
Altitude		
Operating	2.4 km (8000 ft) maximum	
Nonoperating	9.1 km (30,000 ft) maximum	
Shock		
Operating	Withstands half-sine shock pulse of 10 G, peak with 10 ± 3 ms duration	
Nonoperating	Withstands half-sine shock pulse of 40 G, peak with 30 ± 10 ms duration	
Vibration		
Operating	Withstands vibration of 0.051 mm (0.002 in) double amplitude (maximum) in the frequency range of 5 to 50 Hz	
Nonoperating	Withstands vibration of 0.25 G, peak, in the frequency range of 50 to 500 Hz	
Power Requirements		
DC	None	
AC	Input voltage range Single phase Frequency Power consumption	184–256 Vac 47-63 Hz 525 VA typical 700 VA maximum

TM78 Logic Assembly Mechanical Specifications

Height	40 cm (15.75 in)
Width	48.25 cm (19 in)
Depth	27.3 cm (10.75 in)
Weight	5.9 Kg (25 lbs)

H7422 Power Supply
Mechanical Specifications

Height	13.3 cm (5.25 in)
Width	48.25 cm (19 in)
Depth	26.7 cm (10.5 in)
Weight	20.4 Kg (45 lbs)
Data Reliability	Established by error rate of transport as follows:

		GCR	**PE**
Recoverable	Read	1 in 10^9	1 in 10^9
	Write	1 in 10^7	1 in 10^7
Nonrecoverable	Read	1 in 10^{10}	1 in 10^{10}

CHAPTER 2
PROGRAMMING INFORMATION

2.1 INTRODUCTION

This chapter contains the programming information required by a user for a system containing the TM78 formatter. The information applies only to the TM78; programming information for other system units can be found in the applicable documentation.

The TM78 common address space (CAS)is used by the host CPU and the internal microcomputer. The CAS is located within the TM78, but is viewed as an extension to the memory address space of both the host CPU (except for DECsystem-10 and DECSYSTEM-20) and TM78 microcomputer. Within this context, they form a tightly coupled, asymmetrical, multiprocessor system. This chapter defines the manner in which the different processes cooperate.

This chapter also contains information about the use of the TM78 hardware control registers. These registers are used during subsystem initialization and diagnostic testing.

The TM78 GCR/PE tape formatter is a MASSBUS device, and is subject to the same configuration rules as other MASSBUS devices (i.e., up to eight TM78s per bus). Each TM78 may connect with as many as four TU78 tape transports. The MASSBUS controller dictates how the TM78 is accessed by the program. Details of programming the MASSBUS controller and data channel (if any) are not provided.

2.2 NON-DATA TRANSFERS

The non-data transfer interface consists of one command location per tape transport, a status location shared by all transports, and the ATTN bit (Figure 2-1).

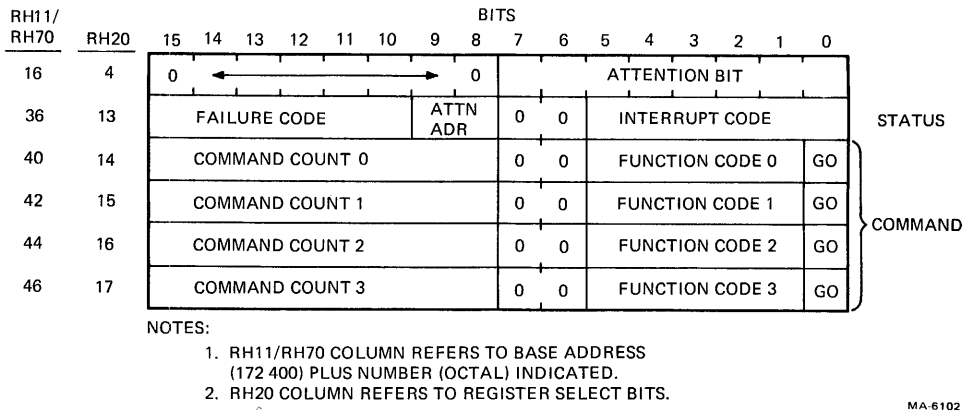


Figure 2-1 Non-Data Transfer Fields

The host CPU may have up to four commands active at any time. The ATTN bit corresponds to the TM78 drive address and is set when a command is completed. Then, the host reads the ATTN ADR to determine the tape unit that has finished, and the Interrupt Code corresponding to the interrupt-level action to take.

If the Interrupt Code indicates a hardware fault condition, then the Failure Code contains additional information for the system error log. To allow for further interrupts, the host CPU must write a logical one into the ATTN Bit after reading the Status location. Command completion interrupts do not necessarily occur in the same order as command initiations.

The Command Count specifies the number of times the command is to be repeated (octal 377 maximum). If the operation terminates prematurely, then the Command Count contains the number of operations not completed successfully. A Command Count of 0 or 1 may be used to specify a single operation.
The TM78 automatically performs all error recovery for non-data transfers. Unrecoverable errors and hardware faults are reported.

The GO bits inform the TM78 that a new command has been loaded. They are not status bits because the readability is undefined.

Non-data transfer function codes and interrupt codes are listed in Tables 2-1 and 2-2, respectively. Table 2-8 cross-references interrupt codes to failure codes.

The Sense command may be used to obtain information about a specific tape transport. This information is available to the user during the time the ATTN bit is set for this command (Figure 2-2).

Sense information is provided primarily for system initialization and error logging. It is not necessary for proper operation during non-error situations.

Table 2-3 lists all the Sense information mnemonics.

2.3 DATA TRANSFERS

The data transfer interface is shared by all four tape transports; therefore, only one transfer may be active at a time. The data transfer command is specified by the Function Code, Record Count, Format, Byte Count, Command Address, and Skip Count. Status information for read/write operations is presented through the Interrupt Code, Byte Count, Record Count, and Failure Code fields (Figure 2-3).

The Function Code and GO bits are loaded after the three locations that define a command. It is not usually necessary to reload registers 2 and 5 in the RH20 (addresses 14 and 6 in the RH11/RH70) in order to repeat an operation (refer to Table 2-5). These locations must not be altered by the host CPU until the operation has finished. Command completion is signaled by a CMD (command done) interrupt in the RH20, and an RDY interrupt in the RH11/RH70. (The attention interrupt is not used for data transfers). The host CPU reads the Interrupt Code to determine which interrupt-level action to take. All Interrupt Codes, except DONE, are accompanied by the DEE bit (drive exception error) in the RH20 and the TRE bit (transfer error) in the RH11/RH70. The CMD ADR specifies the tape unit to be used. This may not be the address of a tape unit for which a non-data transfer command is active.

Table 2-1 Non-Data Transfer Function Codes

Function Code (Go bit included)	Name	Note	Description
03	NO OP		Generate a unique NO OP interrupt code
05	Unload		Unloads tape and interrupts immediately
07	Rewind	4	Rewinds tape and interrupts when done
11	Sense	1	Puts status information into CAS
13	Data Security Erase	2	Erase remainder of tape and rewind
15	WTM PE	3	Writes phase encoded tape mark
17	WTM GCR	3	Writes GCR tape mark
21	SP FWD REC		Spaces forward record, stops if tape mark
23	SP REV REC		Spaces reverse record, stops if tape mark or BOT
25	SP FWD FILE		Spaces forward file (to tape mark)
27	SP REV FILE		Spaces reverse file (to tape mark)
31	SP FWD EITHER		Spaces forward either record or file
33	SP REV EITHER		Spaces reverse either record or file
35	ERG PE	3	Erases three inches of tape, sets PE
37	ERG GCR	3	Erases three inches of tape, sets GCR
41	Close File PE	3	Writes two tape marks, spaces reverse one, sets PE
43	Close File GCR	3	Writes two tape marks, spaces reverse one, sets GCR
45	SPACE LEOT		Spaces forward until two tape marks, spaces reverse one
47	SPACE FWD FILE/LEOT	5	Spaces forward to tape mark, stops if two successive tape marks (logical end of tape)

NOTES

1. Sense registers are valid as long as the ATTN bit is set.
2. Erases at least 3.05 m (10 ft) beyond the EOT marker.
3. Recording format is ignored except when tape is at load point (BOT). It is specified by bit 1.
4. Sometimes interrupts when rewind starts; always interrupts after tape motion has stopped.
5. Do not use after any reverse operation; the TM78 may skip over an LEOT located where direction was reversed.

Table 2-2 Non-Data Transfer Interrupt Codes

Interrupt Code	Name	Description
01	DONE	Operation completed as expected
02	TM	Unexpected tape mark
03	BOT	Unexpected beginning of tape
04	EOT	Tape positioned beyond end of tape marker (write)
05	LEOT	Unexpected logical EOT (two tape marks)
06	NO OP	NO OP completed
07	RWDING	Rewind in progress; DONE interrupt follows when at BOT
10	FPT	Write attempted on file protected tape
11	NOT RDY	TU on-line; tape rewinding or loading, or DSE being performed from other port
12	NOT AVAIL	TU not switched to this port, but is on-line
13	Off Line	TU not switched on-line
14	NON EX	TU does not exist or power is off
15	Not Capable	1. Incorrect ID Burst read 2. No record or tape mark detected
27	Bad Tape	Tape position lost
30	TM FAULT A	TM78 hardware has failed, or the CAS was loaded with incorrect command information (see failure code for details)
31	TU FAULT A	Tape unit hardware has failed (see failure code for details)

RH11/RH70	RH20	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
26	6	1	1	0	0	DUAL MB	1	0	DRIVE TYPE								
20	7	RDY	PRES	ONL	REW	PE	BOT	EOT	FPT	AVAIL	SHR	MAINT	DSE	0	0	0	0
30	10	BCD		SN	3	BCD		SN	2	BCD		SN	1	BCD		SN	0

NOTES:
1. RH11/RH70 COLUMN REFERS TO BASE ADDRESS (172 400) PLUS NUMBER (OCTAL) INDICATED.
2. RH20 COLUMN REFERS TO REGISTER SELECT BITS.

MA-6173

Figure 2-2 Sense Information Fields

Table 2-3 Sense Information

Name	Definition
DUAL MB	When set, TM78 has dual MASSBUS port option
DRIVE TYPE	Octal 101 for TU78 tape drives
RDY	Tape unit has tape mounted, is on-line, and is not rewinding or performing DSE
PRES	Tape unit has power applied
ONL	Tape unit is on-line and tape is mounted
REW	Tape unit is rewinding
PE	When set, tape unit is set for PE recording format; when clear, tape unit is set for GCR recording format
BOT	Tape is positioned at load point
EOT	Tape is positioned beyond end-of-tape marker
FPT	Tape unit is write protected
AVAIL	Tape unit is available to this MASSBUS
SHR	Tape unit is available to both MASSBUS ports (shared)
MAINT	Tape unit is in maintenance mode, and may not be used
DSE	Tape unit is performing erase portion of DSE command
BCD SN	Binary-coded-decimal serial number of the tape unit

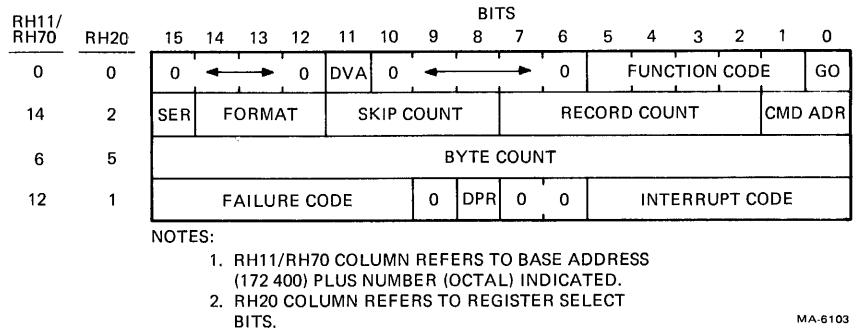


Figure 2-3 Data Transfer Fields

The Record Count specifies the number of records to read or write, and may be any value in the range of 0 to 77_8. When it is not zero, it is decremented after every record correctly transferred. When it is zero, the TM78 transfers records until stopped by the MASSBUS controller. The RH20 has its own block counter and may be operated with the Record Count set to zero. For the RH11/RH70, a block of memory may be divided into multiple records by using the Record Count. Record Count is zero upon a normal termination, and after an error occurs indicates the number of records remaining to be transferred. It is not decremented during unsuccessful error retry operations, so that it does not have to be reloaded after an error, unless the TM78 issues a Read Opposite interrupt code. In this case, the Record Count should be set to zero. When writing, records are always started with byte A (Figure 2-4). Any unwritten bytes in the last word of a buffer are not written in the next record.

The length of the record (or records) to be read or written is determined by the Byte Count. The entire record is always sent to the MASSBUS controller, even if it is longer than Byte Count indicates. If the record length differs from the Byte Count, the actual length is returned in Byte Count, unless the interrupt code is Read Opposite (refer to Table 2-8). In addition, the MASSBUS controller can detect record length errors when the TM78 transfers an unexpected number of bytes to the MASSBUS controller (or channel). A Byte Count of zero implies 2^{16} bytes.

If the TM78 detects an error that requires a retry, it positions the tape for the retry operation unless SER (suppress error repositioning) is set. If SER is not set, error recovery algorithms of the TM78 inform the host CPU of the next operation to perform via the interrupt code. A record is declared unreadable if repeated error recovery attempts fail. If a record cannot be written, the TM78 responds with BAD TAPE (Interrupt Code 27).

The Format field (Figure 2-4) defines the manner in which tape bytes are assembled to/from the host CPU words. Skip Count is used during tape read operations to zero-fill the specified number of byte positions before reading the first data byte. These zero-filled bytes are transferred from the TM78 even if no data bytes are read (because of an error).

2.3.1 Extended Sense (EXSNS) Command

The EXSNS command is used to read error log data from the TM78. This log data should be read and placed into the host system error log file whenever interrupt code host response J is executed (refer to Paragraph 2.8). This command functions in a manner similar to the READ FWD command, except that SER, Format, Skip Count, and Byte Count fields are ignored. The EXSNS command always sends 60_{10} (74_8) bytes of sense data over the MASSBUS data bus in the 11 Normal format. This produces an ordered string of bytes in an RH11, RH70 or RH11/780. In an RH10/20, the CPU word is formatted as shown in Figure 2-5.

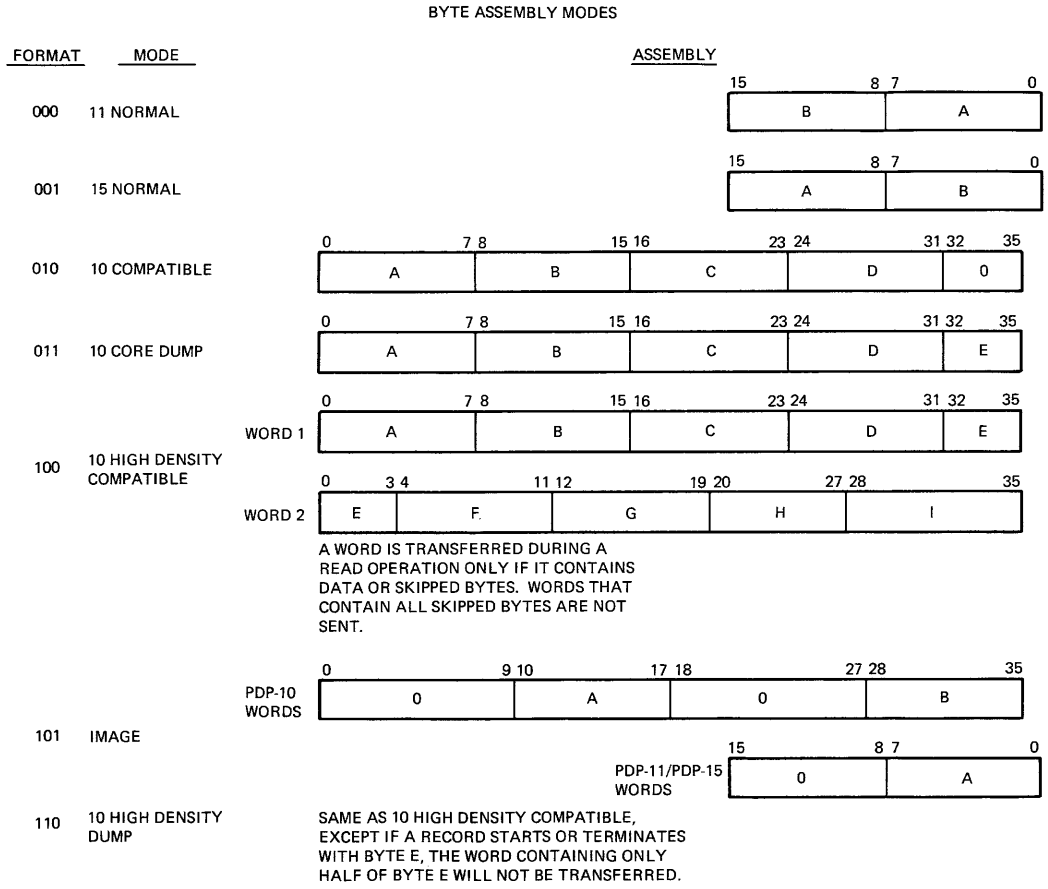
The TM78 maintains separate log data for each of the four possible tape transports. The CMD ADR field selects which set of log data is read. Log data is updated whenever an interrupt code is presented to the host, and one of the following conditions is true.

1. The interrupt code is TM, BOT, EOT, FPT, NOT RDY, NOT AVAIL, Off Line, NON EX, Not Capable, Retry, READ OPP, Unreadable, Error, EOT ERROR, Bad Tape, TM FAULT A, or TU FAULT A.

2. The failure code is not zero.

Both data transfer and non-data transfer errors cause log data to be updated. Log data is never cleared. Refer to Appendix A for a description of the extended sense data bytes.

Data transfer function codes are listed in Table 2-4, and data transfer interrupt codes are listed in Table 2-5.



SKIP COUNTS

SKIP COUNT	11 NORM FWD	11 NORM REV	15 NORM FWD	15 NORM REV	10 COMP FWD	10 COMP REV	10 DUMP FWD	10 DUMP REV	HIGH DENS COMP FWD	HIGH DENS COMP REV	HIGH DENS DUMP FWD	HIGH DENS DUMP REV
0	A	B	A	B	A	D	A	E	A	I	A	I
1	B	A	B	A	B	C	B	D	B	H	B	H
2					C	B	C	C	C	G	C	G
3					D	A	D	B	D	F	D	F
4							E	A	E	E	E*	E**
5									F*	D**	F*	D**
6									G*	C**	G*	C**
7									H*	B**	H*	B**
10									I*	A**	I*	A**

* WORD 1 IS NOT SENT
** WORD 2 IS NOT SENT

NOTES:

THIS CHART INDICATES THE LOCATION OF THE FIRST BYTE READ VERSUS THE SKIP COUNT. SKIPPED BYTES IN THE FIRST WORD CONTAIN ZEROS. UNDEFINED SKIP COUNTS RESULT IN A TM FAULT A INTERRUPT.

MA-6111

Figure 2-4 Byte Assembly Modes and Associated Skip Counts

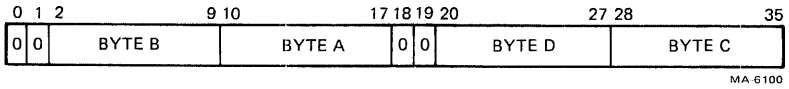


Figure 2-5 RH10/20 EXSNS Data Byte Formatting

Table 2-4 Data Transfer Function Codes

Function Code (Go bit included)	Name	Description
51	WRT CK FWD	Write Check Forward. Tape subsystem reads one record in a forward direction. Data is checked in RH controller.
57	WRT CK REV	Write Check Reverse. Tape subsystem reads one record in a reverse direction. Data is checked in RH controller.
61	WRITE PE*	Write phase encoded records
63	WRITE GCR*	Write group-coded records
71	READ FWD	Read records forward
73	EXSNS	Read extended sense error log
77	READ REV	Read records reverse

*The recording density format is ignored unless the tape is positioned at load point. At load point, the write command specifies the recording format of the entire tape.

Table 2-5 Data Transfer Interrupt Codes

Int Code	Name	Definition	Tape Position	Byte Count	Record Count
01	DONE	READ OR WRITE completed successfully	As expected	No change	0
02	TM	Unexpected tape mark encountered during read operation, otherwise read correctly	After tape mark	No change	Number of records left
03	BOT	Unexpected BOT encountered during read reverse operation, no other errors	At BOT	No change	Number of records left
04	EOT	Write operation successfully completed beyond EOT marker	As expected	No change	Number of records left
10	FPT	Write attempted on file-protected tape	No change	No change	No change
11	NOT RDY	TU is on-line and switched to this port, but is rewinding or loading	N/A	No change	No change
12	NOT AVAIL	TU is on-line, but not switched to this port	No change	No change	No change
13	OFF LINE	TU is not on-line	No change	No change	No change
14	NON EX	TU does not exist, or power is off	No change	No change	No change
15	NOT CAPABLE	1. Incorrect or no ID Burst detected	1. At BOT	No change	No change
		2. No record or tape mark detected	2. Approx. 25 ft from previous position	No change	No change
20	LONG REC	Last record read longer than initial Byte Count value, but otherwise read correctly	After long record	Actual record length	Number of records left

Table 2-5 Data Transfer Interrupt Codes (Cont)

Int Code	Name	Definition	Tape Position	Byte Count	Record Count
21	SHORT REC	Last record read shorter than initial Byte Count value, but otherwise read correctly	After long record	Actual record length	Number of records left
22	RETRY	Error; initial operation should be repeated	Positioned for retry	Initial byte count	Number of records left
23	READ OPP	Read error; initial read should be performed in opposite direction	After bad record	Number of bytes to be read	Number of records left
24	UNREADABLE	Read retries have failed to read record	After bad record	Number of bytes transferred	Number of records left
25	ERROR	Error has occurred which requires a retry but SER is set (excludes length errors)	After bad record	Number of bytes transferred	Number of records left
26	EOT ERROR	Write error has occurred beyond EOT marker, and SER is set	After bad record	Number of bytes transferred	Number of records left
27	BAD TAPE	Tape position has been lost, or write retries have failed to write record	Undefined	Number of bytes transferred	Number of records left
30	TM FAULT A	Hardware has failed, or software bug has been detected. (Failure Code contains more specific information)	Unknown	Unknown	Unknown
31	TU FAULT A	Tape unit has failed (Failure Code contains more specific information)	Unknown	Unknown	Unknown

NOTE

In the above description, the "initial" operation or Byte Count is that of the command before any errors occurred (i.e., the user-specified operation). The "number of records left" is the sum of those records initially specified but not yet accessed and those records accessed but failed because of an unexpected condition.

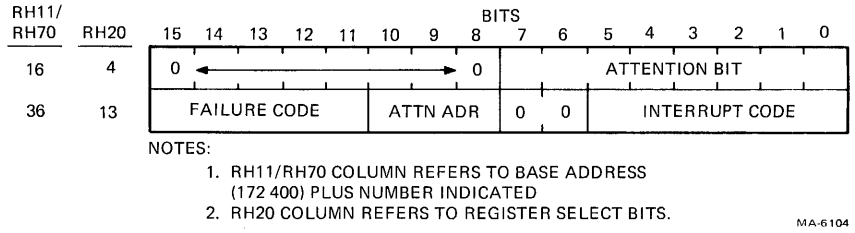


Figure 2-6 TM78 Initiated Interrupt Fields

Table 2-6 TM78 Initiated Interrupt Codes

Code	Name	Note	Definition
17	ON LINE	3	A tape unit has come on-line with a tape loaded or rewinding
32	TM FAULT B	1, 2	The TM78 has detected an internal hardware failure
34	MB FAULT	1, 2	MASSBUS error has occurred

NOTES
1. ATTN ADR is not meaningful.
2. TM CLR operation must be performed.
3. Sense information is valid during the interrupt.

2.4 TM78 INITIATED INTERRUPTS

The TM78 may initiate interrupts to the host CPU under certain conditions that are not the result of commands. Interrupts are sent via the non-data transfer status locations.

An interrupt is initiated by the TM78 when a tape drive comes on-line (Figure 2-6). It is sent to the MASSBUS port (or ports) as determined by the port selection switch in the tape drive. The ATTN ADR indicates which drive has come on-line. (Refer to Paragraph 2.6 for more information about this switch.)

If TM78 internal diagnostics detect a hardware fault during an idle period, a FAULT B interrupt is issued. The Failure Code contains specific information, possibly stored in the system error log, about the nature of the failure. This interrupt is sent to both MASSBUS ports. After a FAULT B interrupt, the TM78 does not respond to commands until a TM CLR (refer to Paragraph 2.5) is issued by the host CPU. Only one FAULT B interrupt can occur during each TM CLR operation. All MB FAULTS are similar, except they are sent only to the port in error.

Table 2-6 lists all the interrupt codes initiated by the TM78.

2.5 TM78 HARDWARE CONTROL REGISTERS

Two registers are implemented to provide a direct path from the MASSBUS to the TM78 hardware. These registers are used for initialization, loading and verification of diagnostic microcode, starting and stopping the microcomputer, and diagnostic access. (Internal addresses are described in Appendix B of the *TM78 Technical Manual.*)

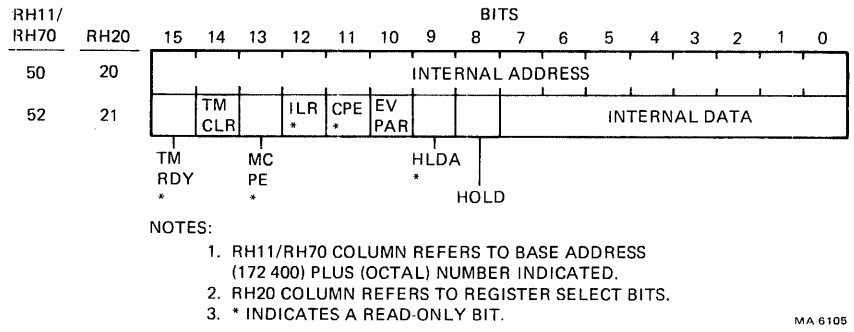


Figure 2-7 TM78 Hardware Control Register Fields

A TM78 may be initialized by a MASSBUS INIT or by setting TM CLR (Figure 2-7). In either case, microcomputer terminates any commands previously loaded. New commands may not be loaded until TM RDY is set; this occurs after microcode initialization. The Drive Type register is valid only when TM RDY is set. TM CLR turns itself off after a short time, and may be considered write-only.

The microcomputer may be stopped by setting the Hold bit.

The stopped condition is indicated by the hold acknowledged (HLDA) bit after a small delay. The microprogram may be continued by clearing Hold.

NOTE

Clearing Hold may set MC PE. Therefore, a TM CLR or MASSBUS INIT should be performed afterward.

The internal MB SEL bit must be loaded before restarting (initializing) from the HOLD state. A MASSBUS INIT clears Hold, but TM CLR does not (except for this difference, the two functions are identical within the TM78). When HLDA is set, the internal address structure of the TM78 may be accessed via Internal Address and Internal Data. If HLDA is not set, the Internal Address contains the current internal address asserted by the microcomputer.

NOTE

When HLDA is not set, Internal Address bits are constantly changing. The contents, therefore, may be undefined, or a parity error may be detected by the MASSBUS controller.

Once HLDA is asserted, Internal Address may be loaded with the address of the location to be accessed. The location is read or written by Internal Data.

The remaining four bits indicate situations that may interfere with proper communication between the microcomputer and the host CPU. They are listed and defined in Table 2-7.

Table 2-7 TM78 Hardware Control Register Error Bits

Name	Definition
MC PE	Microcomputer ROM parity error has occurred
ILR	Reference has been made to nonexistent MASSBUS register address
CPE	Parity error detected as a result of write to some MASSBUS register address
EV PAR	Diagnostic bit causes even parity to be generated and checked for on the MASSBUS control bus

ILR and CPE also cause MB FAULT interrupt. The interrupt occurs when the microcomputer notices the error, which may be some time after the bit actually sets.

2.6 DUAL PORT

One or two MASSBUSes may be connected to a TM78. The DUAL MB sense bit indicates dual port hardware. Each TU78 tape transport can be switched to either zero, one, or both ports. These conditions are indicated by the MAINT, AVAIL and SHR sense bits. A tape unit is always available (AVAIL) if DUAL MB hardware is not installed.

NOTE

If the dual port option is not present, the tape unit is AVAIL when the TU78 port select switch is in any position except MAINT.

All four bits (DUAL MB, AVAIL, SHR and MAINT) are intended for system configuration purposes and error logging. If a port attempts to use a tape unit not switched to it, a NOT AVAIL interrupt is generated.

The TM78 makes no attempt to synchronize a shared tape unit between operations from two ports. If two commands are active at one time, they are executed in an unpredictable sequence. Interrupts are returned to the MASSBUS that issued the command, except FAULT B and On-Line, which return to both MASSBUSes in a shared configuration. It is expected that if two separate processes are sharing a tape unit, they have an external path of resource-sharing intercommunication. Synchronization is performed through this external path.

Processes not synchronized should never read a shared tape. Not only will records be received in random order, but error recovery operations may fail. Records may be written in an unsynchronized fashion only if ordering is not important.

The TM78 does not respond to the MASSBUS port request sequence used by some other MASSBUS devices.

2.7 CHANNEL ADDRESS SUMMARY

RH11 and RH70 addresses, relative to the TM78, are summarized in Figure 2-8. RH10, RH20, and RH780 addresses, relative to the TM78, are summarized in Figure 2-9.

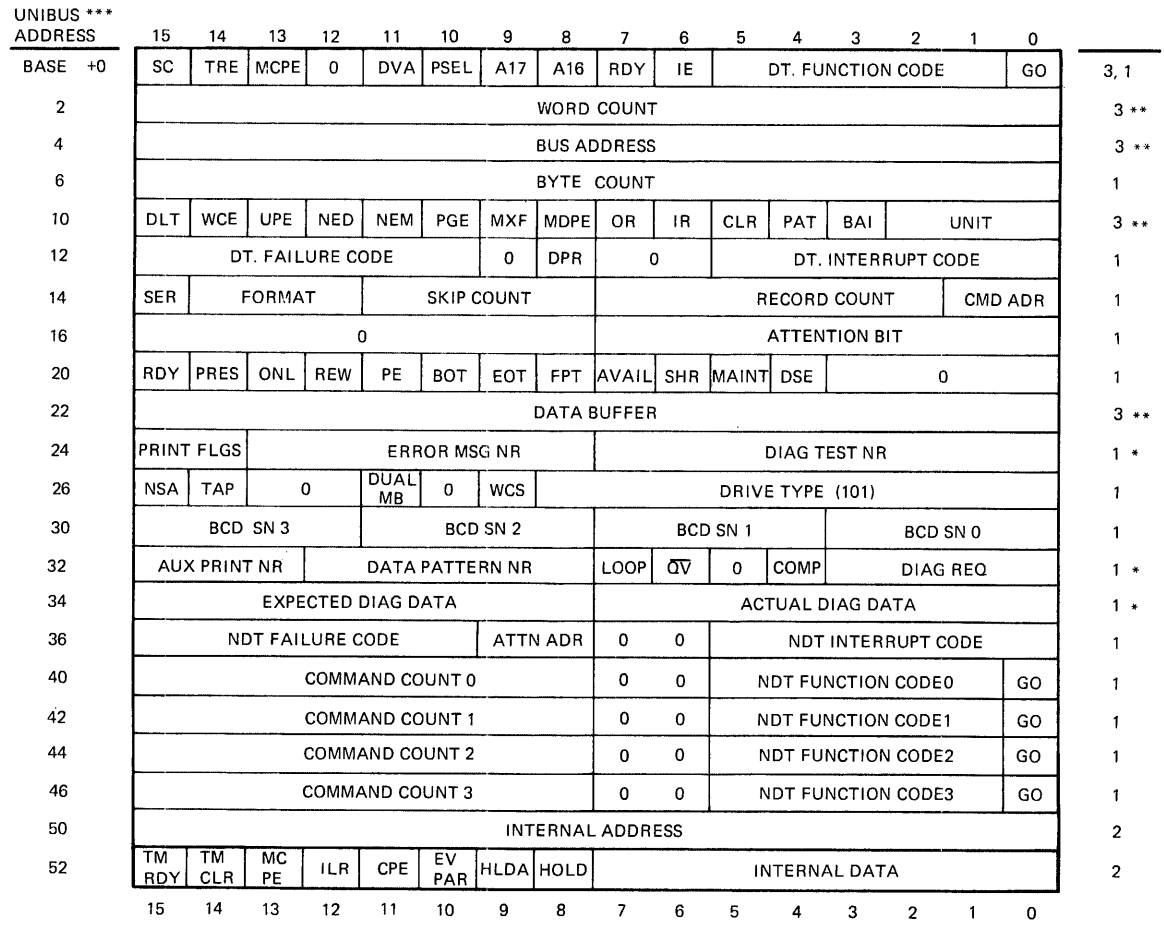


Figure 2-8 RH11 and RH70 Address Summary

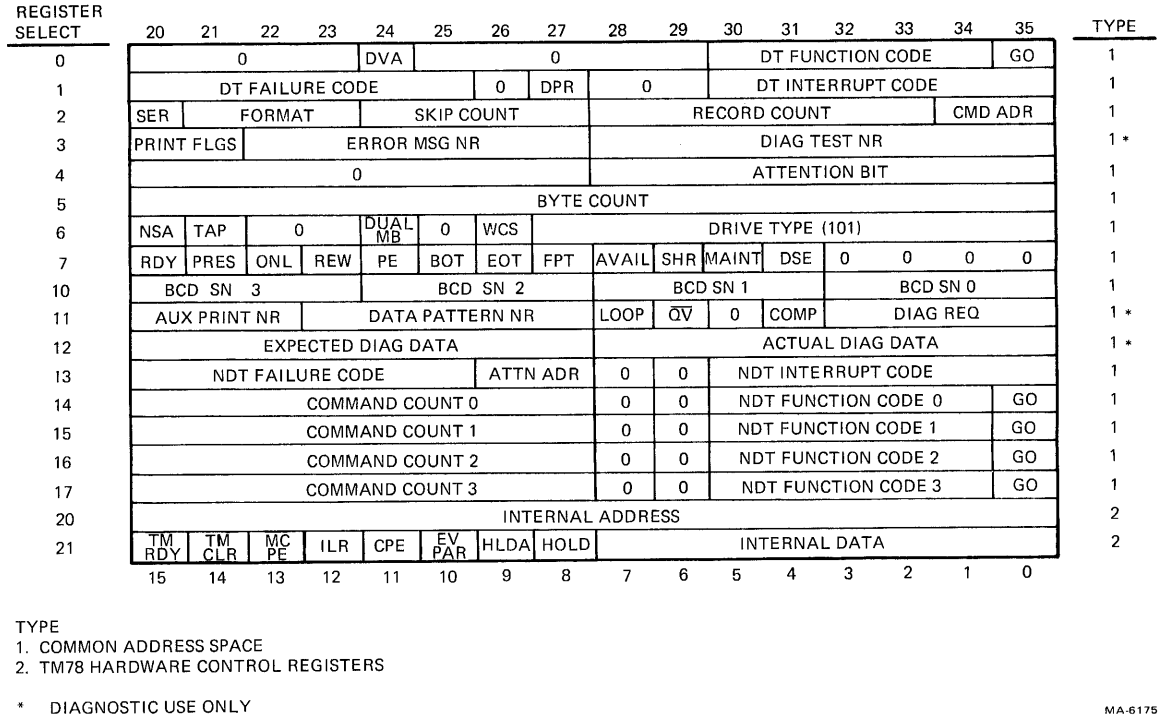


Figure 2-9 RH10, RH20, and RH780 Addresses

2.8 INTERRUPT CODE FAILURE CODE CROSS-REFERENCE AND SUMMARY

The tables which follow summarize the contents of this chapter. The list below describes each table.

Table	Description
2-8	Interrupt Code to Failure Code
2-9	Non-data Transfer (NDT) Interrupts to NDT Commands
2-10	Data Transfer (DT) Interrupts to DT Commands
2-11	TM78 Initiated Interrupts
2-12	Host Responses

Table 2-8 Interrupt Code to Failure Code

Int Code	Name	Use	Failure Code
01	DONE.	NDT or DT	00 – Extended sense data not updated
			01 – Extended sense data updated and contains something of interest
02	TM	NDT or DT	Always zero
03	BOT	NDT or DT	01 – Command was issued with tape at BOT
			02 – Saw BOT indicator after tape motion started
			03 – ARA ID detected
04	EOT	NDT or DT	00 – Extended sense data not updated
			01 – Extended sense data updated and contains something of interest
05	LEOT	NDT	Always zero
06	NO OP	NDT	Always zero
07	REWINDING	NDT	Always zero
10	FPT	NDT or DT	Always zero
11	NOT RDY	NDT or DT	01 – TU is on-line but not ready (Possible when TU is manually rewound or loading)
			02 – Fatal error has occurred and this command cannot be performed until error status has been presented and a TM CLEAR received
			03 – Access to TU is allowed but TU is either rewinding or doing a DSE from another MASSBUS or keypad command
12	NOT AVAIL	NDT or DT	Always zero
13	OFF LINE	NDT or DT	Always zero
14	NON EX	NDT or DT	Always zero
15	NOT CAPABLE	NDT or DT	01 – No record found within 25 ft (7.6 m) of tape
			02 – ID Burst neither PE or GCR
			03 – ARA ID not found
			04 – No GAP found after ID Burst (PE) or ARA ID Burst (GCR)

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code
17	ON LINE	TM INIT	Always zero
20	LONG REC	DT	00 – Extended sense data not updated
			01 – Extended sense data updated and contains something of interest
21	SHORT REC	DT	00 – Extended sense data not updated
			01 – Extended sense data updated and contains something of interest
22	RETRY	DT	01 – CRC error, ACRC error, pointer mismatch, uncorrectable or two track error set in ECCSTA register (This code generated by write GCR operations)
			02 – CRC error, ACRC error or uncorrectable set in ECCSTA register (This code generated by read GCR operations)
			03 – Uncorrectable error set in ECCSTA register (This code generated by read PE operations)
			04 – AMTIE, pointer mismatch, uncorrectable, two track error or single track error set in ECCSTA register (This code generated by write PE operations)
			05 – At least one bit set in ECCSTA register
			06 – At least one Write Fail bit set in RPFAIL and RPATH registers (This code generated by write PE operations)
			07 – More than one Write Fail bit set in RPFAIL and RPATH registers (This code generated by write GCR operations)
			10 – RSTAT contains bad code
			11 – CRC characters from WMC and RMC do not match (This code generated by write PE operations)
			12 – MASSBUS data bus parity error
			13 – Record length incorrect during retry opposite attempt; invalid data has been transferred
23	READ OPP	DT	Same as Int Code 22
24	UNREADABLE	DT	Same as Int Code 22

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code
25	ERROR	DT	Same as Int Code 22
26	EOT ERROR	DT	Same as Int Code 22
27	BAD TAPE	NDT or DT	Same as Int Code 22
30	TM FAULT A	NDT or DT	01 – Illegal command code
			02 – Data transfer command issued while non-data transfer command in progress on same tape unit
			03 – WMC error; check Encode register for reason. May be Illegal Format or Skip Count codes
			04 – RUN not received from MASSBUS controller
			05 – Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated in selected function routine)
			06 – ECC ROM parity error
			07 – XMC ROM parity error
			10 – Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Verify ID Burst command loaded during write of BOT area)
			11 – Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Verify ARA Burst command loaded during write of BOT area)
			12 – Command read from RMC register RCMDP did not match command loaded into RCMD register (This code generated when Verify ARA ID command loaded during write of BOT area)
			13 – Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Verify Gap command loaded during write BOT area)

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code		
			14	–	Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Read ID Burst command loaded during read of BOT area)
			15	–	Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Verify ARA ID command loaded during read of BOT area)
			16	–	Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Verify Gap command loaded during read of BOT area)
			17	–	Command read from RMC register RCMLP did not match command loaded into RCMD register (This code generated when Find Gap command loaded during Erase Gap routine)
			20	–	WMC LEFT failed to set in Extended Sense routine
			21	–	XL PE set in INTSTA register
			22	–	XMC DONE did not set
			23	–	WMC ROM PE or RD PE set in WMCERR register
31	TU FAULT A	NDT or DT	01	–	TU Status parity error
			02	–	TU Command parity error
			03	–	Rewinding tape went off-line
			04	–	Tape went not ready during DSE
			05	–	TU CMD status changed during DSE
			06	–	TU velocity never came up to speed
			07	–	TU velocity changed after up to speed and writing started
			10	–	TU CMD did not load correctly to start tape motion in selected function routine
			11	–	TU CMD did not load correctly to set drive density

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code
			12 – TU CMD did not load correctly to start tape motion to write BOT ID Burst
			13 – TU CMD did not load correctly to backup tape to BOT after failing to write BOT ID
			14 – Failed to write density ID Burst correctly
			15 – Failed to write ARA Burst correctly
			16 – Failed to write ARA ID correctly
			17 – ARA error bit set in MTA Status B register
			21 – Could not find a gap after the ID code was written correctly
			22 – TU CMD did not load correctly to start tape motion to read ID Burst
			23 – Time-out looking for BOT after detecting ARA ID Burst
			24 – Failed to write Tape Mark correctly
			25 – Tape never came up to speed while trying to reposition for retry of writing Tape Mark
			26 – TU CMD did not load correctly to start tape motion in Erase Gap routine
			27 – Could not detect a gap in Erase Gap routine
			30 – Could not detect a gap after writing record
			31 – Read path terminated before entire record was written
			32 – Could not find a gap after writing record and read path terminated early
			33 – TU CMD did not load correctly to backup for retry of Write Tape Mark
			34 – TU velocity changed after up to speed while trying to reposition for retry of writing Tape Mark
			35 – TU CMD did not load correctly to backup to retry a read of BOT ID
			36 – Time-out looking for BOT after failing to write BOT ID

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code		
			37	–	TU velocity changed while writing PE gap before starting to write record
			40	–	TU CMD did not load correctly to set PE tape density at start of write BOT ID Burst
			41	–	TU CMD did not load correctly to set GCR tape density after writing Density ID
			42	–	TU CMD did not load correctly to set PE tape density at start of read from BOT
			43	–	TU CMD did not load correctly to set GCR tape density after reading a GCR Density ID Burst
32	TM FAULT B	TM INIT	00	–	RST0 interrupt occurred with TM RDY still set
			01	–	Power failed to interrupt
			02	–	Interrupt for unknown reason on channel 5.5
			03	–	Interrupt for unknown reason on channel 6.5
			04	–	Interrupt for unknown reason on channel 7
			05	–	Interrupt for unknown reason on channel 7.5
			06	–	CAS contention retry count expired
			07	–	CAS Contention error not retryable
			10	–	Queue error; could not find queue entry
			11	–	Queue entry already full
			12	–	8085 ROM parity error
			13	–	In-line test 0; WMC self test failed = M8959-M8957
			14	–	In-line test 1; XMC ROM parity error M8958-M8959-M8960
			15	–	In-line test 2; RPM self test failed M8953-M8960
			16	–	In-line test 3; RPM1 channel 0 self test failure M8950 (slot AB12)
			17	–	In-line test 4; RPM1 channel 1 self test failure M8950 (slot AB13)

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code		
			20	–	In-line test 5; RPM1 channel 2 self test failure M8950 (slot AB14)
			21	–	In-line test 6; RPM1 channel 3 self test failure M8950 (slot AB15)
			22	–	In-line test 7; RPM1 channel 4 self test failure M8950 (slot AB16)
			23	–	In-line test 10; RPM1 channel 5 self test failure M8950 (slot CD13)
			24	–	In-line test 11; RPM1 channel 6 self test failure M8950 (slot CD14)
			25	–	In-line test 12; RPM1 channel 7 self test failure M8950 (slot CD15)
			26	–	In-line test 13; RPM1 channel P self test failure M8950 (slot CD16)
			27	–	In-line test 14; RPM1 error correction self test M8950-M8951-M8953
			30	–	In-line test 15; 40000-40777 RAM memory failure M8960
			31	–	In-line test 16; 41000-41777 RAM memory failure M8960
			32	–	In-line test 17; 42000-42777 RAM memory failure M8960
			33	–	In-line test 20; 43000-43777 RAM memory failure M8960
			34	–	In-line test 21; 44000-44777 RAM memory failure M8960
			35	–	In-line test 22; 45000-45777 RAM memory failure M8960
			36	–	In-line test 23; 46000-46777 RAM memory failure M8960
			37	–	In-line test 24; 47000-47777 RAM memory failure M8960
			40	–	In-line test 25; loop write to read at TU port 0 – GCR
			41	–	In-line test 26; loop write to read at TU port 0 – PE

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code		
			42	–	In-line test 27; loop write to read at TU port 1 – GCR
			43	–	In-line test 30; loop write to read at TU port 1 – PE
			44	–	In-line test 31; loop write to read at TU port 2 – GCR
			45	–	In-line test 32; loop write to read at TU port 2 – PE
			46	–	In-line test 33; loop write to read at TU port 3 – GCR
			47	–	In-line test 34; loop write to read at TU port 3 – PE
			50	–	In-line test 35; loop write to read at MTA 0 – GCR
			51	–	In-line test 36; loop write to read at MTA 0 – PE
			52	–	In-line test 37; loop write to read at MTA 1 – GCR
			53	–	In-line test 40; loop write to read at MTA 1 – PE
			54	–	In-line test 41; loop write to read at MTA 2 – GCR
			55	–	In-line test 42; loop write to read at MTA 2 – PE
			56	–	In-line test 43; loop write to read at MTA 3 – GCR
			57	–	In-line test 44; loop write to read at MTA 3 – PE
34	MB FAULT		01	–	Control bus parity error
			02	–	Illegal register referenced

Table 2-8 Interrupt Code to Failure Code (Cont)

Int Code	Name	Use	Failure Code		
77	KEY FAIL		01	–	Keypad entry error
			02	–	TM78 not off-line
			03	–	Illegal instruction code
			04	–	Microdiagnostic start or continue command issued
			05	–	Microdiagnostic loop on error command issued

Table 2-9 Non-Data Transfer (NDT) Interrupts to NDT Commands

NDT Interrupt	Possible NDT Commands	Host Response*
DONE	Any except NO OP	A
TM	SP FWD REC, SP REV REC	B
BOT	SP REV REC, SP REV FILE, SP REV EITHER	B, O
EOT	WTM PE, WTM GCR, ERG, Close File	C
LEOT	SP FWD FILE/LEOT	D
FPT	WTM PE, WTM GCR, ERG, Close File, DSE	E
NOT RDY	Any except NO OP and Sense	F
NOT AVAIL	Any except NO OP and Sense	G
OFF LINE	Any except NO OP and Sense	H, F
NON EX	Any except NO OP and Sense	G
NO OP	NO OP	A
BAD TAPE	Any except NO OP, Sense, DSE, Rewind, Unload	I, J, G
TM FAULT A	Any	J, G
TU FAULT A	Any	J, G
REWINDING	Rewind	U
NOT CAPABLE	Any space command	G, T

*See Table 2-12

Table 2-10 Data Transfer (DT) Interrupts to DT Commands

DT Interrupt	Possible DT Commands	Host Response*
DONE	Any	A
EOT	Write PE, Write GCR	C
LONG REC	Read Fwd, Read Rev	L, K
SHORT REC	Read Fwd, Read Rev	L
RETRY	Any with SER=0	M
READ OPP	Read Fwd, Read Rev with SER=0	P
NOT CAPABLE	Read Fwd, Read Rev	G, T
UNREADABLE	Read Fwd, Read Rev with SER=0	I, J
BAD TAPE	Any with SER=0	I, J, G
ERROR	Any with SER=1	N
EOT ERROR	Write PE, Write GCR with SER=1	N
TM	Read Fwd, Read Rev	B
BOT	Read Rev	B, O
FPT	Write PE, Write GCR	E
NOT RDY	Any	F
NOT AVAIL	Any	G
OFF LINE	Any	H, F
NON EX	Any	G
TM FAULT A	Any	J, G
TU FAULT A	Any	J, G

*See Table 2-12

Table 2-11 TM78 Initiated Interrupts

TM Interrupt	Host Response*
ON LINE	S
TM FAULT B	J, R
TU FAULT B	J, R
MB FAULT	J, R

*See Table 2-12

Table 2-12 Host Responses

Host Response	Meaning
A	Return "operation complete"
B	Stop any look-ahead buffering; Return "end of file reached"
C	Return "end of tape" error (Never rely on the physical relationship between EOT and record location, since this can change between units)
D	Return "logical end of tape", or other appropriate action
E	Return "illegal write"
F	Retry operation after receiving a TM78 initiated interrupt for that tape unit
G	Return "device error"
H	Inform operator of condition
I	Return "data error"
J	Enter Failure Code in the system error log
K	Return "record is longer than user requested"
L	Set "incorrect record length" status; Obtain actual size from Byte Count location
M	Repeat previous operation, starting at record in error
N	User performs his/her own error recovery algorithm, if any
O	Set "beginning of tape" status

Table 2-12 Host Responses (Cont)

Host Response	Meaning
P	Read opposite 1. Use Record Count to dequeue any records which were correctly transferred. Load Record Count with 0. 2. Byte Count now contains the TM78 best guess of the actual record length. Use this value to recompute the memory buffer address and Skip Count. Byte Count does not need to be reloaded. If record does not fit in buffer, compute number of words for data channel to skip, or perform response I. 3. Issue READ FWD or READ REV command. Use command opposite the initial direction before any errors occurred. 4. Follow correct response to resulting interrupt code. The TM78 returns a DONE or possibly a SHORT REC interrupt code when record is correctly read and positioned in memory.
R	Issue a TM CLEAR, unless retry count exceeded; Reissue all commands for which interrupts have not been received, Update retry count
S	Continue any processes that were waiting for this tape unit
T	Invoke tape labeling procedure for handling blank tape
U	Flag the tape unit as busy; Expect a future done interrupt

CHAPTER 3
INSTALLATION

3.1 SITE PLANNING AND CONSIDERATIONS

Since the TM78 is always contained within a transport cabinet, site planning is accomplished when the cabinet is considered. The additional power required to supply the TM78 is 700 W.

3.2 UNPACKING

Likewise, there are no unpacking instructions for the TM78 because it is mounted inside the master transport cabinet. The TM78 cables may be shipped separately and are the only items that must be unpacked.

3.3 INSPECTION

Perform inspection of the TM78 according to the following procedures.

1. Check that the TM78 is securely mounted to the frame members inside the transport cabinet. Ensure that there is no apparent damage to the backplane (cracks, bent pins, etc.).

2. Remove the four 10-32 screws (Figure 3-1) securing the left side of the TM78 gate, and swing it out on its hinge. Loosen the two logic cover retaining screws (Figure 3-2), and remove the cover.

3. Check that all circuit modules are firmly seated in their correct locations (Figure 3-3).

4. Replace the logic cover, and tighten the retaining screws.

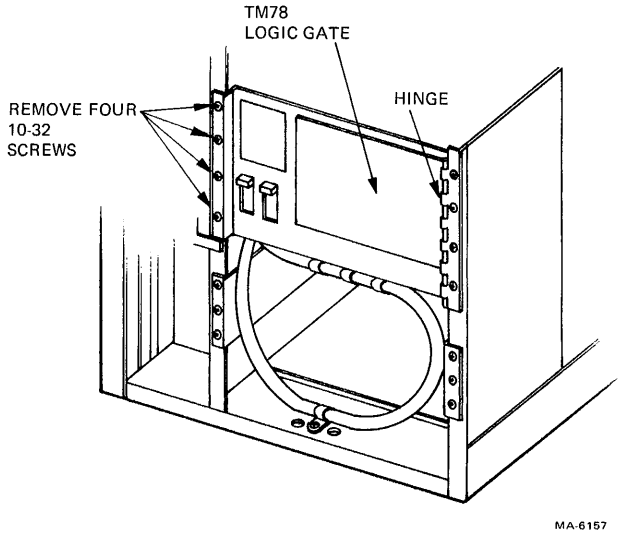


Figure 3-1 Releasing TM78 Logic Gate

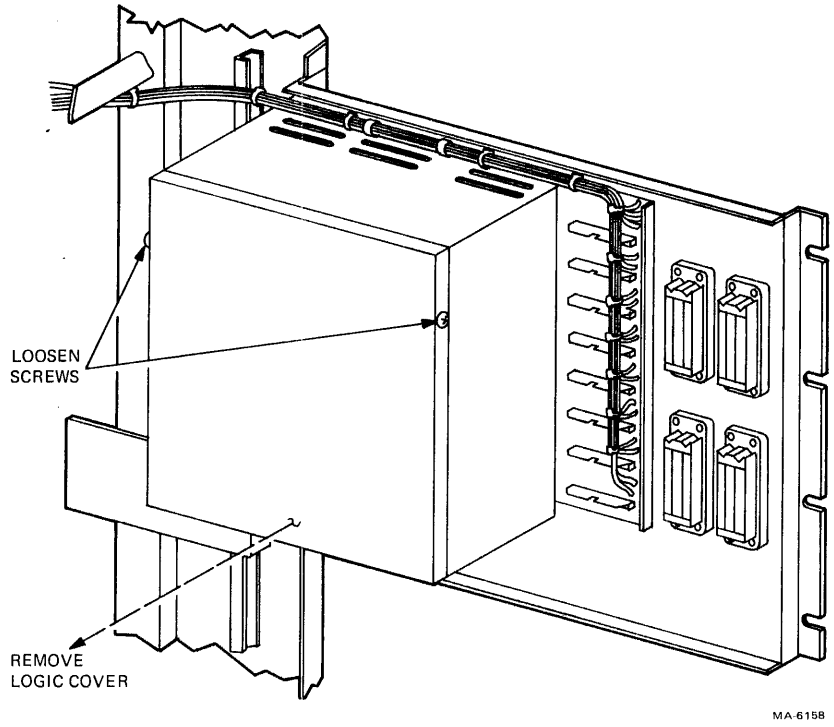


Figure 3-2 Removing TM78 Logic Cover

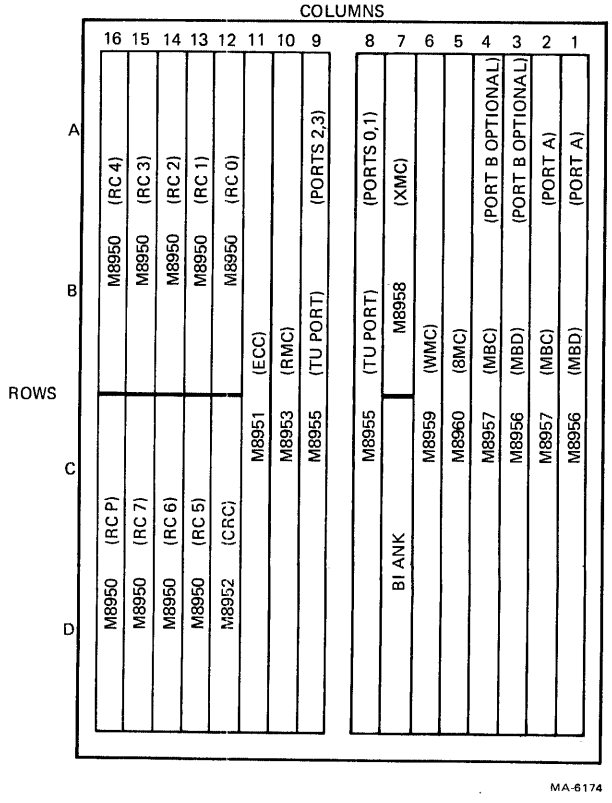


Figure 3-3 TM78 Module Layout

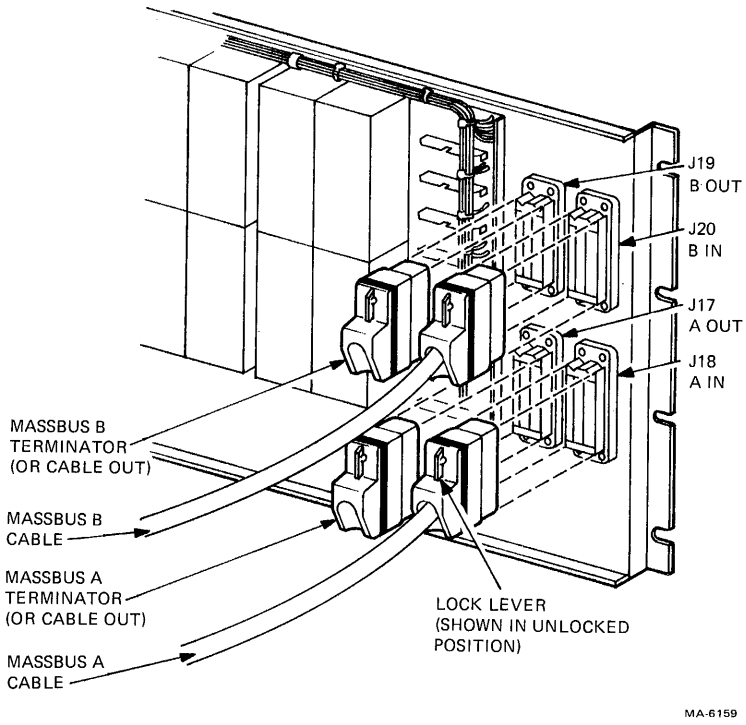


Figure 3-4 MASSBUS Cable Terminator Connections

3.4 INSTALLATION PROCEDURES

Installation consists of cabling as many as four BC06S cables to the TM78. The number of cables depends upon the number of MASSBUS ports and whether additional MASSBUS devices are to be connected to the same MASSBUS controller. A dual ported TM78 may require field installation of dual port logic. Paragraph 3.4.3 describes the procedures for installing the dual port logic. Installation also comprises setting the appropriate TM78 drive address(es).

NOTE
If the TM78 cables are already installed, omit the steps outlined in Paragraphs 3.4.1 and 3.4.2.

3.4.1 MASSBUS Cabling

Perform the installation of MASSBUS cabling according to the following procedures.

1. Connect one end of the 25 ft (7.6 m) MASSBUS cable to the port A input jack (J18) at the rear of the logic gate assembly (Figure 3-4).

2. Lock the connector in place by turning the lock lever 90 degrees clockwise to a horizontal position.

3. If no other MASSBUS device is to be connected, terminate the cable by plugging the MASSBUS terminator provided (PN 70-09938) into the port A output jack (J17).

4. Position the MASSBUS cable as shown in Figure 3-5, and secure it to the logic gate and frame assembly with the six cable clamps and hardware provided.

5. Connect the opposite end of the MASSBUS cable to the distribution panel at the rear of the host computer system.

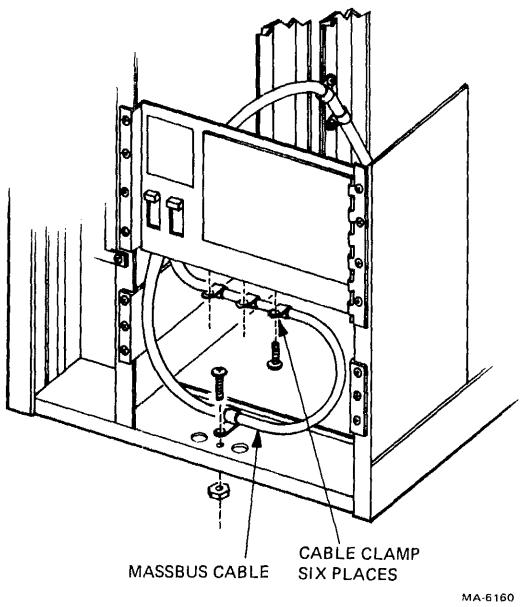


Figure 3-5 MASSBUS Cable Routing and Hardware

3.4.2 TU Bus Cabling

The radial tape unit bus is made up of two flat cables (P/N 70-17382-15). Figure 3-6 shows how these cables are routed electrically. Note that each transport has a unique set of cables, and the jacks to which they are connected (on the TM78) determine the unit number. Figure 3-7 shows the physical placement of the cables within the TM78. To route the cable pair, first remove two cable retainers. Then, the cables are formed and laid, and the retainers are replaced. If there are multiple cable pairs, the pair for the highest tape unit number must be installed first, and the pair for the lowest tape unit number installed last. In other words, work from jack J8 toward jack J1 so that all cables lay flat. Place the connectors so that the colored stripes on the cables are toward the MASSBUS jacks.

For information on cable routing in the transport, refer to the installation chapter in the *TU78 User Guide.*

3.4.3 TM78-C Optional Dual Port Logic

A master dual port TU78/TM78 subsystem may be shipped from the factory as a single port subsystem, with dual port logic in a separate container. Or an existing single port master may be upgraded to dual port at a later date in the field. In either case, the procedure below must be followed in order to create a dual-ported master.

1. Inspect the contents of the upgrade kit. The following system-tested components should be included: one M8956 MASSBUS data module, one M8957 MASSBUS control module, one 25 ft MASSBUS cable, and one MASSBUS terminator.

2. Gain access to the logic cage by following the steps in Paragraph 3.3.

3. Insert the M8956 and M8957 modules into backplane slots 3 and 4, respectively (Figure 3-4).

4. Replace the logic cover.

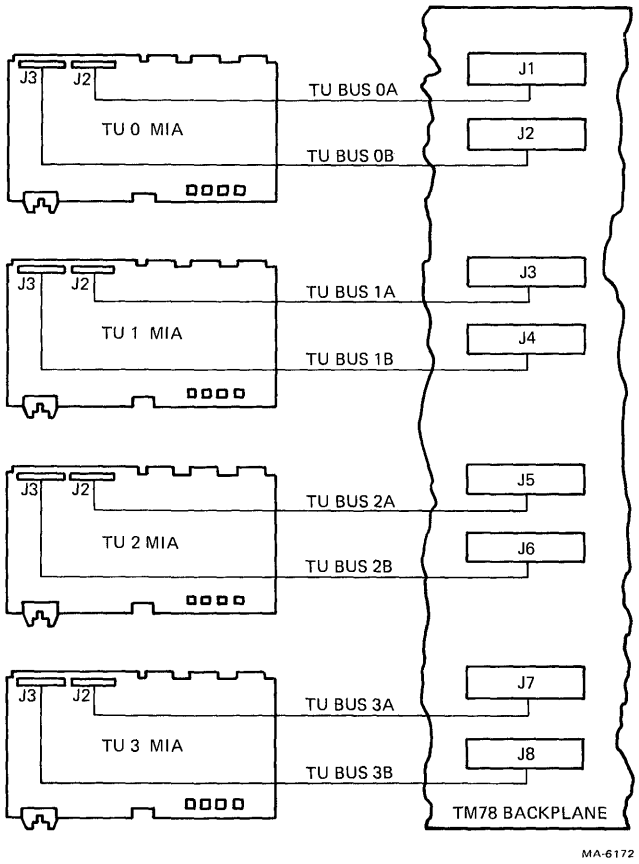


Figure 3-6 Radial TU Bus Connections

5. Follow the steps in Paragraph 3.4.1 for running the MASSBUS cable, and connect it to the port B input jack (J20). Connect the cable terminator to the port B output jack (J19) (Figures 3-4 and 3-5).

6. Connect the opposite end of the MASSBUS cable to the distribution panel at the rear of the host computer system.

7. Set the port B drive address switches (Paragraph 3.4.4).

8. Verify the integrity of the dual port logic by running the appropriate control logic diagnostic from the computer connected to port B.

3.4.4 Setting MASSBUS Drive Address

The drive address for both MASSBUS ports is set into a small DIP switch mounted on the TM78 backplane. (Refer to Figure 1-5 for the location of this switch.) Figure 3-8 shows the eight individual switches contained within the DIP switch and their functions. Locate the three address-determining switches for the appropriate MASSBUS port. The three switches (A2:0) form a 3-bit binary field for a maximum of eight drive addresses. To set an address bit, press the switch in on the left side (1 side). To clear an address bit, press the switch in on the right side. Thus, for drive address 0, all three would be set to 0; for drive address 1, only A0 would be set to 1, and so on.

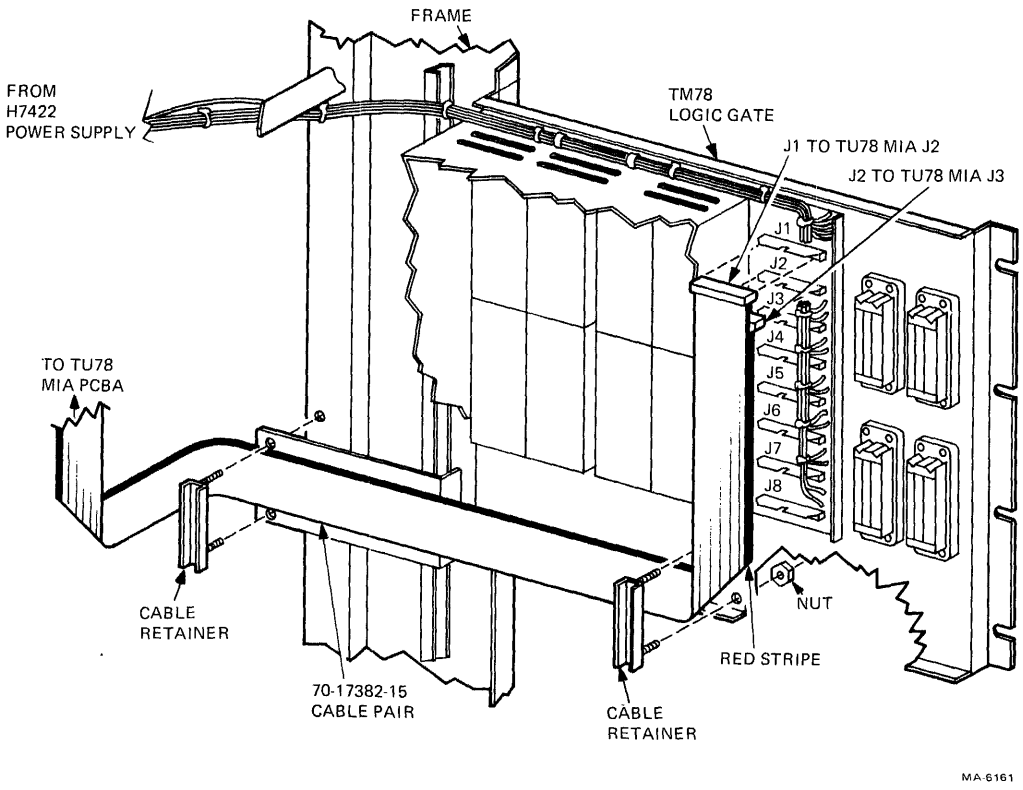


Figure 3-7 TU Bus Cable Routing and Hardware

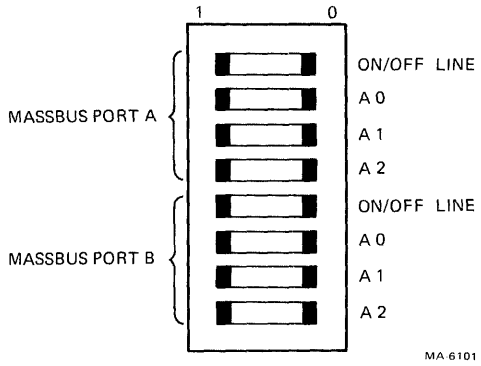


Figure 3-8 MASSBUS Port A/B Drive Address Selector Switch

The on/off-line switches are used for maintenance purposes only. To electrically remove one or both ports of a drive from the host system(s), push the appropriate switch in on the right side. The normal position for these switches is the on-line, or left position. Taking one of two ports off-line does not necessarily mean that a given transport is off-line; the transport may be switched to the opposite port through its control panel port selector switch.

NOTE

If the dual port option (port B) is not present in the TM78, the lower set of four switches has no effect.

3.5 ACCEPTANCE TESTING

The TM78 acceptance tests are run concurrently with the master TU78 acceptance tests. Refer to the subsystem acceptance procedures found in Paragraph 3.5 of the *TU78 User Guide* or *TU78 Technical Manual.*

APPENDIX A
EXTENDED SENSE COMMAND (73) DATA BYTES

BYTE	DESCRIPTION
1.	Command code being executed on last error
2.	Interrupt code from last error
3.	Failure code from last error
4.	Hardware register 0; read path write fail bits
5.	Hardware register 1; read path diagnostic bits
6.	Hardware register 2; read path status
7.	Hardware register 3; read path command loop
8.	Hardware register 20; AMTIE
9.	Hardware register 21; RC DONE
10.	Hardware register 22; illegal 5-4
11.	Hardware register 23; mark 2
12.	Hardware register 24; end mark
13.	Hardware register 25; RC PAR bits
14.	Hardware register 26; postamble det
15.	Hardware register 27; data
16.	Hardware register 30; CRC
17.	Hardware register 31; corrected data
18.	Hardware register 32; ECC status
19.	Hardware register 40; channel 0 TIE bus
20.	Hardware register 41; channel 1 TIE bus

BYTE	DESCRIPTION
21.	Hardware register 42; channel 2 TIE bus
22.	Hardware register 43; channel 3 TIE bus
23.	Hardware register 44; channel 4 TIE bus
24.	Hardware register 45; channel 5 TIE bus
25.	Hardware register 46; channel 6 TIE bus
26.	Hardware register 47; channel 7 TIE bus
27.	Hardware register 50; channel P TIE bus
28.	Hardware register 60; TIE bus
29.	Hardware register 104; AMTIE
30.	Hardware register 110; PORT status
31.	Hardware register 114; read data
32.	Hardware register 240; CAS status
33.	Hardware register 241; CBUS status
34.	Hardware register 300; DBUS status
35.	Hardware register 320; WMC status
36.	Hardware register 321; TU select 0
37.	Hardware register 322; TU select 1
38.	Hardware register 323; write data
39.	Hardware register 324; byte counter <7:0>
40.	Hardware register 324; byte counter <15:8>
41.	Hardware register 325; PAD counter <7:0>
42.	Hardware register 325; PAD counter <15:8>
43.	Hardware register 326; ECODE counter <7:0>
44.	Hardware register 326; ECODE counter <15:8>
45.	Hardware register 330; DDR/MBD A

BYTE	DESCRIPTION
46.	Hardware register 331; DDR/MBD B
47.	Hardware register 332; WMC errors
48.	Hardware register 340; interrupt status
49.	MIA register 0; TU78 status
50.	MIA register 1; MIA status A
51.	MIA register 2; MIA status B
52.	MIA register 3; serial NR A
53.	MIA register 4; serial NR B
54.	MIA register 5; TU diag
55.	Retry counter (RETCNT). This byte is the count of retry interrupt requests given for the tape unit. When this count is zero, the tape unit is not in a retry sequence.
56.	Retry control bits (RETCNT+1). This byte is used by the microcode to control error recovery. It is meaningful only when the retry counter (byte 55) is not zero. Bit 5 – set when initial command moved in the reverse direction Bit 6 – set when initial command was a read Bit 7 – set when last retry requested was in opposite direction of initial command
57.	TU software status (TUx). This byte contains information about the tape drive. Bit 0 – set when a data security erase command is in progress Bit 1 – set when a rewind command is in progress Bit 2 – set when tape unit exists and power is on Bit 3 – set when a non-data transfer command issued from a MASSBUS port is in progress Bit 4 – set when tape was last moved in the reverse direction Bit 5 – set when last tape operation involved writing on tape Bit 6 – set when last record seen was a tape mark Bit 7 – set when last MASSBUS command came from port B

BYTE	DESCRIPTION
58.	Transfer control word (XFRCTL). This byte contains control information used by data transfer commands. Bits 0-2 – write clock select Bits 3-5 – read clock select Bit 6 – PLO bypass Bit 7 – low read threshold
59.	Retry suppress and format control (XRETRY). This byte contains the contents of the left half of the MASSBUS register, which contains the retry suppress bit, format, and skip count.
60.	Keypad enable flag (ENAON). This byte is not zero when the keypad is enabled.

NOTE

The contents of bytes 4 through 48 are described in Appendix B of the TM78 Technical Manual. The contents of bytes 49 through 54 are described in Appendix C of the TM78 Technical Manual.

TM78 MAGNETIC TAPE FORMATTER
USER GUIDE
EK-0TM78-UG-001

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